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PTO/SB/08A (08-00)

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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete if Known

Application Number	10/743894
Filing Date	12/17/2003
First Named Inventor	Madurawe, Raminda U.
Group Art Unit	2819
Examiner Name	D. de
Attorney Docket Number	

Sheet 1 of 2

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
he		4,706,216		Carter	11-10-1987	
		4,870,302		Freeman	09-26-1989	
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Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ³
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		Application Number	10/774,389/
		Filing Date	12/17/2003
		First Named Inventor	Madurawe, Raminda U.
		Group Art Unit	2819
		Examiner Name	D. Le
		Attorney Docket Number	
Sheet	2	of	2

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Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
he		SEALS & WHAPSHOTT, "Programmable Logic – PLDs and FPGAs", 1997, pp 102-117, McGraw-Hill, USA.	<input type="checkbox"/>
w		ASHOK K. SHARMA, "Programmable Logic Handbook – PLDs, CPLDs, & FPGAs", 1998, pp 99-171, McGraw-Hill, USA.	<input type="checkbox"/>
he		E. AHMED, J. ROSE, "The Effect of LUT and Cluster Size on Deep-Submicron FPGA Performance and Density", FPGA 2000, Monterey, CA, 2000.	<input type="checkbox"/>
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